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Characteristics of Si^+ / B^+ dual implanted silicon wafers①

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[Abstract] Thin p^+ layers with good electrical properties were fabricated by RTA (rapid thermal annealing) with post-FA (furance annealing) of Si^+ / B^+ dual implanted silicon wafers. The electrical and structural characteristics of thin p^+ layers have been measured by FPP (four-point probe), SRP (spreading resistance probe), RBS/channelling. Optimizing the implantation and annealing processes, especially using the thermal cycle of RTA followed by FA, shallow p^+ n junctions can be fabricated, which shows excellent I-V characteristics with revers-bias leakage current densities of 1.8 nA/cm^2 at − 1.4 V.

[Key words] rapid thermal annealing; dual ion implantation; silicon thin p^+ layers
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1 INTRODUCTION

For silicon-photo-diodes (SPD), it is necessary to form shallow p^+ n junctions with very low reverse-bias leakage current densities. To form thin p^+ layers, both the doping and annealing steps must be optimized. Ion implantation steps must be taken to eliminate ion channelling[1], either by pre-amorphizing the surface layer[2, 3] or by using a heavy molecular ion beam such as BF_2^+, $B_{10}H_{14}$[4, 5]. Diffusion can be limited when short annealing time or lower temperature is applied. RTA is very effective for dopant to have high activation and low redistribution[6~ 7].

This paper shows that thin p^+ layers with excellent electrical properties can be produced by Si^+ / B^+ dual implantation and RTA followed by FA. It just contrasts with Ref. [8], in which the author revealed that only the thermal cycle of FA followed by RTA can fabricate the shallow p^+ n junctions with good characteristics.

2 EXPERIMENTAL

Phosphorus-doped (0.8~ 1.2 Ω•cm) CZ n-type (100) silicon wafers were used throughout this work. Implantation parameters for p^+ layers were listed in Table 1. Two sets of Si^+ pre-amorphization were employed: the first, thin amorphous layer, i. e. 40 keV Si^+ pre-implantation to a dose of 3.0×10^{15} cm^{-2}, producing an amorphous layer about 100 nm thick; the second, thick amorphous layer, i. e. 80 keV Si^+ pre-implantation to doses of 1.5×10^{15} cm^{-2} and 3.0×10^{15} cm^{-2}, producing an amorphous layer about 140 nm and 210 nm thick, respectively. After amorphization of the surface, all the wafers were implanted with 20 keV B^+ to a dose of 5.0×10^{14} cm^{-2}. A single-implantation control wafer was prepared by an implantation of 20 keV B^+ ions to a dose of 5.0×10^{14} cm^{-2}. Implantation was performed at a tilt angle of 7° on a water-cooled target. All wafers underwent rapid isochronous annealing at temperatures ranging from 800 ℃ to 1 150 ℃ for 20 s or rapid isothermal annealing at 1 100 ℃ for 5~ 60 s in dry N_2 ambient.

The SPD with a junction area of 2 500 μm × 3 000 μm, with the same RTA conditions and implantation parameters as above studies, was fabricated by a special process. The diodes fabricated with B^+ single implantation were performed to compare with the Si^+ / B^+ dual implantation diodes.

The carrier concentration depth profiles were measured by SRP technique. SRP, in conjunction with FPP measurements of sheet resistance, can also provide information about the degree of dopant activation. The depths of amorphous layers, the crystal quality, and the residual damage were characterized by RBS/ion channelling.

3 RESULTS AND DISCUSSION

Fig. 1 shows carrier concentration depth profiles. The junction depth X_j is not greater than 0.24 μm in all cases except for B^+ single implantation, where X_j = 0.38 μm. For sample No. SB3, after 1 100 ℃, 30 s RTA, the junction depth is 0.18 μm and the sheet resistance R_s = 80 Ω/ □. SRP, in conjunction with FPP, also provides that about 97% boron atoms are activated after RTA at 1 100 ℃ for 30 s, while

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Table 1 Implantation parameters

No.	Ion	Energy/ keV	Dose/ cm^{-2}	Dose rate/ ($\mu A\cdot cm^{-2}$)
B1	B^+	20	5.0×10^{14}	0.19
SB1	Si^+ / B^+	40/ 20	$3.0\times10^{15}/5.0\times10^{14}$	0.39/ 0.17
SB2	Si^+ / B^+	80/ 20	$1.5\times10^{15}/5.0\times10^{14}$	0.39/ 0.17
SB3	Si^+ / B^+	80/ 20	$3.0\times10^{15}/5.0\times10^{14}$	0.39/ 0.17

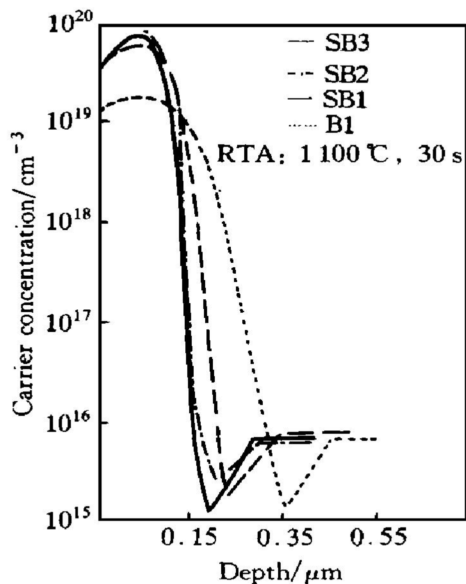

Fig. 1 Carrier concentration depth profiles after RTA at 1 100 ℃ for 30s

the activation degree is only 37% for B^+ single implantation wafer. Therefore the optimization of dual implantation parameters and RTA conditions must be taken to form a thin p^+ layers with good quality.

Because of the high degree of dopant activation, from the carrier concentration depth profiles in Fig. 1, we can also observe the diffusion of boron as functions of annealing time and temperature in crystalline and Si^+ preamorphized substrates. There is a very fast diffusion in the crystalline wafer (sample No. B1), perhaps due to interstitial processes; but in Si^+ / B^+ dual implantation wafers, the RTA deeply eliminates the diffusion.

The production of sharp implanted dopant profiles is strongly dependent on the nature of the amorphized region. Ion energy, ion dose, ion species and the substrate temperature are very important variables in the formation of amorphous layers. RBS/ ion channelling spectra (Fig. 2) shows the influence of some of these variables on the amorphization of silicon substrates and annealing. For example, the 80 keV Si^+ implantation to a dose of 1.5×10^{15} cm^{-2} at water-cooled target temperature yielded an 140 nm thick amorphous layer. For Si^+ / B^+ dual implantation wafers, RBS/ ion channelling data show that an initial damage (amorphous) peak is eliminated while some residual damage still remains after RTA at 1 100 ℃ for 15 s or longer. In the same time, we should note

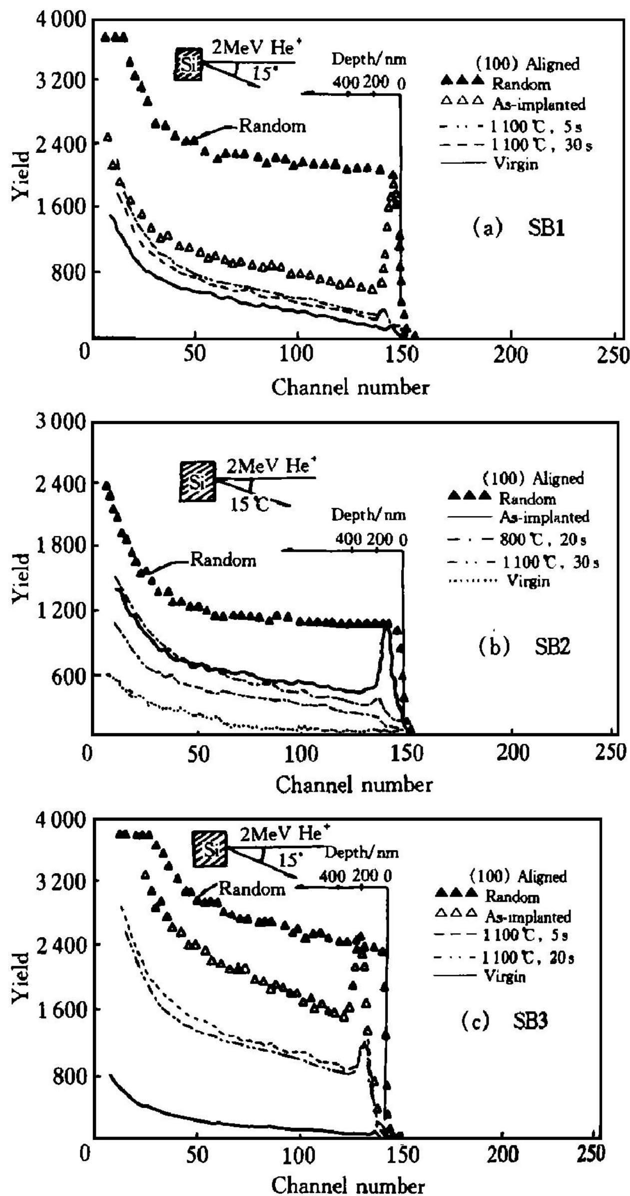

Fig. 2 (100) aligned RBS channelling spectra for Si^+ / B^+ dual implanted samples

that high dose B^+ single implantation induced damage is much more difficult to anneal out[6].

The effects of the implantation parameters and annealing conditions on the reverse-bias leakage current density J are also investigated. Post-FA (800 ℃, 20 min) has effectively reduced the reverse-bias leakage current. Annealing methods do not affect the bulk component of leakage current, while RTA will increase the surface component. The reason for this phenomenon may be that bulk g-r (generation-

recombination) centers in the Si/SiO_2 interface layer near p^+ n junction and/or interface state densities will increase after RTA, while post-FA can eliminate them. The leakage current density of sample No. SB3 is about 3 orders of magnitude higher than that of sample No. SB1 and possesses the same order of magnitude as that of sample No. SB2. The smallest reverse leakage current density (No. SB1) is 1.8 nA/cm^{-2} at − 1.4 V. These results show that Si^+ / B^+ dual implantation parameters must be optimized and Si^+ / B^+ dual implantation and RTA combined with post-FA technique can be applied to fabricate silicon-photo-diodes with shallow p^+ n junctions, while B^+ single implantation or only FA will induce much deeper junction and greater leakage current.

4 CONCLUSIONS

Both RTA and pre-amorphization are required to form thin p^+ layers. The induced damage which was produced by Si^+ / B^+ dual implantation can be removed by RTA. Si^+ preamorphization can effectively inhibit the Boron channelling effect. RTA combined with post-FA and Si^+ / B^+ dual implantation can be used to fabricate silicon-photo-diodes with good electrical characteristics, while B^+ single implantation or Si^+ / B^+ dual implantation then only FA will form much thick p^+ layers.

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